GW4235

Low Power Energy Harvest with MPPT

1 Description

GW4235 is a microlight collection management charging chip that integrates power management, charge/discharge management, and energy storage device management. The GW4235 can achieve cold start with energy input as low as 400mV and 15μW of power, and after startup, it can obtain DC power from light conversion devices such as solar panels, charge energy storage devices such as rechargeable batteries or supercapacitors, and provide stable operating voltage for different loads through two LDO regulators.

2 Features

- Ultra-low power start-up: cold start can be realized under 400mV input voltage and 15μW input power.
- Boost regulator: MPPT can be configured through pins, which can be configured as 70%, 75%, 85% or 90%; the MPPT open circuit voltage is detected every 5 seconds; the input voltage range is 150mV to 5V after startup.
- Low-voltage LDO output: support a maximum load current of 20mA; output voltage 1.2V/1.8V optional; switch control through pins.
- High-voltage LDO output supports a maximum load current of 80mA; the output voltage is optional/adjustable from 1.8V to 4.2V; it can be controlled by pins.
- Battery management: configure overcharge and over discharge protection parameters for rechargeable batteries or supercapacitors; prompt when the battery is exhausted; prompt when LDO is available.
- Battery switching: When the energy storage battery is exhausted, it will automatically switch to the primary battery; when the energy storage battery recovers, it will automatically switch to the energy storage battery.

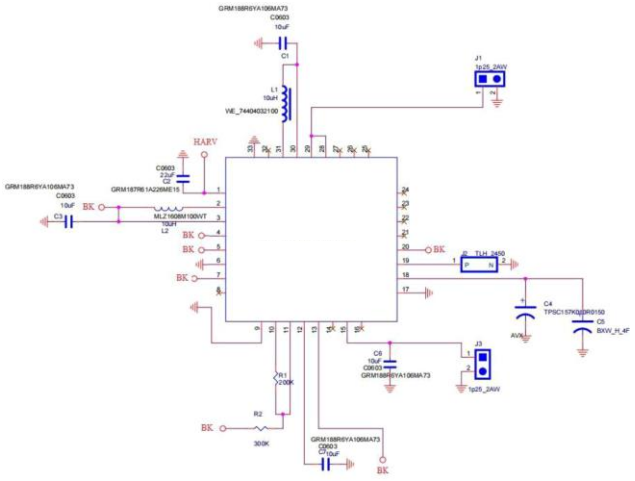
3 Physical Characteristics

- Operating voltages
  - Input voltage:
    - Cold start: 0.4V to 5V
    - After cold start: 0.15V to 5V
  - Output voltage:
    - Boost converter: 2.2V to 4.5V
    - Buck converter: 2V to 2.5V
  - Energy storage device voltage:
    - Rechargeable Batt.: 2.2V to 4.5V
    - Capacitance: 0V to 4.5V
- Operating junction temp.: -40°C to 125°C

4 Typical Applications

- Industrial Monitoring
- Home Automation
- Electronic Health Monitoring
- Industrial Internet of Things
- Wireless Sensor Nodes

5 Basic Application Diagram



6 Ordering Information

Device name	Package	Remark
GW4235IRTVT	5.0mmx5.0mm, 0.5mm pitch	QFN32, Tray
GW4235IRTVR	5.0mmx5.0mm, 0.5mm pitch	QFN32, Tape&Reel

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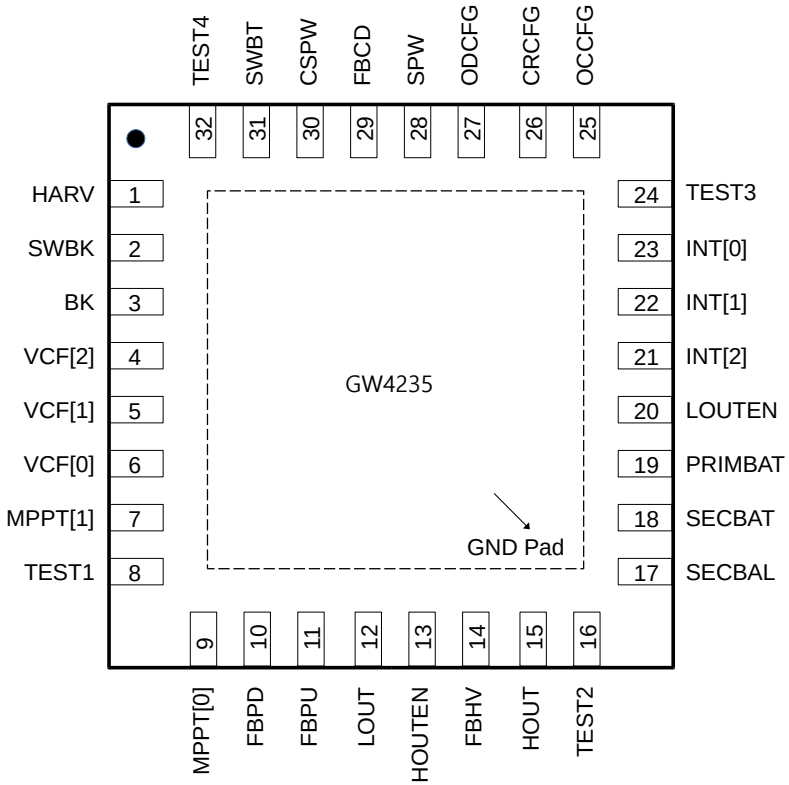
7 Revision History

Version	Date	Description
0.1	October 30, 2024	Preliminary release

8 Pin Configuration and Function



Pin Functions

Pin Name	No.	Description
HARV	1	The output of the boost converter
SWBK	2	Switch Node of Buck Converter
BK	3	The output of the buck converter
VCF[2]	4	Used to configure the threshold voltage of the energy storage element and the output voltage of the LDO
VCF[1]	5	Used to configure the threshold voltage of the energy storage element and the output voltage of the LDO
VCF[0]	6	Used to configure the threshold voltage of the energy storage element and the output voltage of the LDO
MPPT[1]	7	For MPPT ratio
TEST1	8	Debug pins need to be left floating
MPPT[0]	9	For MPPT ratio
FBPD	10	Configuration for primary battery (optional), must be connected to GND if not used
FBPU	11	Configuration for primary battery (optional), must be connected to GND if not used
LOUT	12	Low-voltage LDO regulator
HOUTEN	13	Enable pin for high voltage LDO
FBHV	14	Used in custom mode for high voltage LDO configuration. Leave unconnected if not used
HOUT	15	The high voltage LDO regulator
TEST2	16	Debug pins need to be left floating
SECBAL	17	Connect to the midpoint of the dual-battery supercapacitor (optional), must be

Pin Name	No.	Description
		connected if not used to GND
SECBAT	18	Connect to energy storage elements, batteries or capacitors, not floating
PRIMBAT	19	Connect to primary battery (optional), must be connected to GND if not used
LOUTEN	20	Enable pin for low voltage LDO
INT[2]	21	Logic output, asserted when the chip performs MPPT calculations
INT[1]	22	Logic output, when the battery voltage is lower than V_{OD} or the chip is getting energy from the primary battery time set
INT[0]	23	Logic output, LDO can be enabled when asserted
TEST3	24	Debug pins need to be left floating
OCCFG	25	In custom mode (optional) used to configure the threshold voltage of the energy storage element, if not used, it must be left unconnected
CRCFG	26	In custom mode (optional) used to configure the threshold voltage of the energy storage element, if not used, it must be left unconnected
ODCFG	27	In custom mode (optional) used to configure the threshold voltage of the energy storage element, if not used, it must be left unconnected
SPW	28	Connect to input energy source
FBCD	29	Configuration for cold start (optional), if not used, must be connected to SPW
CSPW	30	Connect to external capacitor buffered boost converter input
SWBT	31	Switching Node of Boost Converter
TEST4	32	Debug pins need to be left floating
GND	Bottom exposed solder plate	Should be firmly connected to the PCB ground plane

9 Specifications

9.1 Absolute Maximum Ratings

Parameter	Rating	Unit
VSPW	5.5	V
Operation Junction Temperature	-40 to +125	°C
Storage temperature	-65 to +150	°C

9.2 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Decoupling Capacitors for SPW Input Pins	C_{SPW}	8	10	150	μF
HARV Converter capacitor	C_{HARV}	10	22	25	μF
HARV Converter inductor	L_{HARV}	4	10	25	μH
BK Converter capacitor	C_{BK}	8	10	22	μF
BK Converter inductor	L_{BK}	4	10	25	μH

Parameter	Symbol	MIN	TYP	MAX	Unit
Decoupling Capacitors for Low Voltage LDOs	C_{LVOL}	8	10	14	μF
Decoupling Capacitors for High Voltage LDOs	C_{HOL}	8	10	14	μF
When the energy storage element is not connected, the SECBAT tube Capacitors configured at pins (optional)	C_{SECBAT}	150			μF
Resistor for setting battery Threshold voltage in custom mode, RT=R1+R2+R3+R4 (optional)	RT	1	10	100	MΩ
Used to set high pressure in custom mode LDO voltage, RV=R5+R6 (optional)	RV	1	10	40	MΩ
Cold start configuration resistor, RC=R9+R10 (can be selected)	RC	0.1		10	MΩ
Primary battery configuration resistor, RP=R7+R8 (can be selected)	RP	100		500	KΩ
High voltage LDO enable pin	HOUTEN Logic high (VOH) Logic low (VOL)	 1.75 -0.01	 V_{BK} 0	 V_{BK} 0.01	 V V
LDO enable pin	LOUTEN Logic high (VOH) Logic low (VOL)	 1.75 -0.01	 V_{BK} 0	 V_{BK} 0.01	 V V
For MPPT Configuration pins	MPPT[1:0] Logic high (VOH) Logic low (VOL)	 Connect to BK Connect to GND			
Configuration tubes for energy storage elements foot	VCF{2:0} Logic high (VOH) Logic low (VOL)	 Connect to BK Connect to GND			

9.3 Typical Electrical Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input power required for cold start	PSPWCS	During cold start	15	-		μW
input voltage	VSPW	During cold start	0.4		5	V
		After cold start	0.15		5	V
Input Current	ISPW				100	mA
Custom cold start voltage	VCS	During cold start	0.5		4	V
Boost converter output voltage	V_{BT}	During normal work	2.2		4.5	V
Buck converter output voltage	V_{BK}	During normal work	2	2.2	2.5	V
Energy storage device voltage	V_{BAT}	Rechargeable battery	2.2		4.5	V
		Capacitor	0		4.5	V
After INT[1] takes effect to shutdown time	T_{DLY}		400	600	800	ms
Primary battery voltage	VPRIMBAT		0.6		5	V
Primary battery output current	IPRIMBAT			20		mA
The minimum charge of primary battery feedback pressure level	V_{FBPU}		0.15		1.1	V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Before disabling the boost converter, the storage the maximum voltage acceptable on the element	V_{OC}		2.3		4.5	V
Enable the LDO after a cold boot before, the minimum voltage required on the energy storage element	V_{CR}		2.25		4.45	V
Before switching to the primary battery or entering the shutdown state, the minimum acceptable energy storage element voltage	V_{OD}		2.2		4.4	V
Low voltage LDO output voltage	V_L		1.2		1.8	V
Load current of low voltage LDO	I_L		0		20	mA
High voltage LDO output voltage	V_H		1.8		Min(V_{BAT} -0.3,4.2)	V
Load current of high voltage LDO	I_H		0		80	mA
Logic output status pin	INT[2:0]	Logic high (VOH)	1.98	V_{BAT}		V
		Logic low (VOL)	-0.1		0.1	V

10 Functional Description

10.1 Deep-sleep and Wake-up Modes

In deep sleep mode, all nodes are deeply discharged, and no available energy is collected by the chip. When the SPW pin meets the 400mV cold-start voltage and 15μW power input, the chip is activated into wake-up mode and the voltages of V_{BT} and V_{BK} rise to 2.2V, and then the voltage of V_{BT} alone rises to V_{OC}. During the cold-start process both LDOs are internally deactivated with no outputs. In the case of an ultracapacitor acting as a storage element, the storage element may need to be charged from 0V.

The boost converter will be fed by the input source. The boost converter will charge the SECBAT through the input source. During the charging of the SECBAT node, both LDOs are disabled. When V_{BAT} reaches V_{CR}, the circuit enters normal mode, and the user can activate or deactivate the outputs of the LDOs using the LOUTEN and HOUTEN pins controls. In the case where the battery is used as a storage element, if its voltage is below V_{CR}, it is first necessary to charge the storage element until the voltage reaches V_{CR}. When V_{BAT} exceeds V_{CR}, the circuit re-enters normal mode.

10.2 Normal Mode

When the chip enters the normal mode, the following three situations may occur:

(1) The power provided by the input source is equivalent to the load power, V_{BAT} is kept between V_{OD} ~ V_{OC}, and the circuit remains in normal mode.

(2) The power provided by the input source exceeds the power consumed by the load, V_{BAT} gradually exceeds V_{OC}, and the circuit enters the overvoltage mode.

(3) The power provided by the input source is lower than the power consumed by the load, V_{BAT} gradually drops below V_{OD}, and the circuit will enter shutdown mode, if a primary battery is connected to the PRIMBAT, the circuit will enter primary battery charging mode

10.3 Boost / Buck

The boost converter raises the voltage available at the input source to a level suitable for charging the energy storage element, which is available at the HARV pin at a voltage V_{BT} in the range of 2.2V to 4.5V. The matching components of this converter are the external inductor LHARV and the capacitor CHARV. V_{BT} is available at the HARV pin, and the matching components for this converter are the external inductor LHARV and the capacitor CHARV. The energy storage element is connected to the SECBAT pin at voltage V_{BAT}, and the battery is short-circuited to the HARV node in normal mode ($V_{BAT} = V_{BT}$). During light energy harvesting, the boost converter will provide a current that is shared between the battery and the load. At the same time, the GW4235 supports charging the energy storage element via a primary battery, charging V_{BAT} to V_{CR}. During this process, PRIMBAT is connected to CSPW and the SPW input pin is disconnected.

A buck converter steps down the voltage from V_{BT} to a constant V_{BK} value of 2.2V, which is available through the BK pin. The supporting components for the buck converter are the external inductor LBK and capacitor CBK .

10.4 LDO Output

The chip has two LDOs to provide different operating voltages:
A high-voltage LDO powers the load through HOUT. This regulator supplies a voltage (V_H) on HOUT with a maximum current of 80mA . In built-in configuration mode, an output voltage of 1.8V , 2.5V , or 3.3V can be selected. It can be adjusted from 2.2 V to V_{BAT} -0.3 V in custom configuration mode . The HOUT output can be dynamically enabled or disabled via logic control pin HOUTEN.

A low-voltage LDO powers the load through LOUT. The regulator supplies 1.8 V or 1.2 V on LOUT (V_L) with a maximum current of 20mA. The LOUT output can be dynamically enabled or disabled via logic control pin LOUTEN.

Table 10-1 shows four possible configurations:

LOUTEN	HOUTEN	LV Output	HV Output
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

10.5 Overvoltage Mode

When VBAT reaches VOC, the charging is completed, and the internal logic part keeps the VBAT voltage value near VOC with a hysteresis of several millivolts to prevent damage to the energy storage element and internal circuits. In this configuration, the boost converter is periodically activated to maintain VBAT and the output of the LDO is still available.

10.6 Primary Battery Mode

When V_{BAT} drops below V_{OD}, the circuit compares the voltage on PRIMBAT to the voltage on FBPU, to determine if a charged primary battery is connected to the PRIMBAT. The voltage on the FBPU is set by two optional resistors, if the voltage on the PRIMBAT divided by 4 is higher than the voltage on the FBPU, the circuit considers the primary battery available and the circuit enters primary power mode. In this mode, the primary battery is connected to CSPW, which becomes the input source of the chip, and the chip remains in this mode until V_{BAT} reaches V_{CR}. When V_{BAT} reaches V_{CR}, the circuit enters normal mode. If primary batteries are not used in the application, PRIMBAT, FBPU, and FBPD must be connected to GND. When using primary battery mode, the CSPW capacitor should be 150μF

10.7 Shutdown Mode

When V_{BAT} drops below V_{OD} and the primary battery fails to supply power, the circuit will enter shutdown mode to prevent damage to the energy storage element and LDO instability caused by deep discharge. Both LDO regulators remain enabled. If the primary battery is not used, the load can be interrupted by a low-to-high transition of INT[1] regardless of whether the load is powered by LOUT or HOUT . If energy from the input source is available and V_{BAT} returns to V_{CR} within T_{DLY} (about 600ms), the chip returns to normal mode. However, if V_{BAT} does not reach V_{CR} after T_{DLY}, the circuit enters deep sleep mode, LDO is disabled, and SECBAT is disconnected from HARV to avoid battery damage due to over-discharge. After this, the chip will have to perform the wake-up procedure described in the Deep-sleep and wake-up modes section.

10.8 Maximum Power Point Tracking (MPPT)

MPPT (Maximum Power Point Tracking) block during transitions between normal mode, shutdown mode and wake-up mode. The MPPT module receives and maintains the information of V_{MPP}, and the sampling is performed approximately every 5 seconds. The GW4235 supports any V_{MPP} level in the range of 0.05V to 5V. It provides selection of four values for V_{MPP} /V_{OV} (input source open circuit voltage) through configuration pin MPPT[1:0]

Tabel 10-2 shows MPPT pin configuration

MPPT[1]	MPTT[0]	V_{MPP} / V_{OV}
1	1	70%
1	0	75%
0	1	85%
0	0	90%

10.9 Balun Dual Cell Supercapacitor

A balun circuit allows the user to balance the internal voltages in a two-cell supercapacitor to avoid damage to the supercapacitor due to excessive voltage on one cell. If SECBAL is connected to GND, the balun circuit is disabled and the balun circuit is disabled. This configuration must be used if a single-cell supercapacitor is connected across SECBAT. If the SECBAL is connected to the node between two cells of the supercapacitor, the balun circuit compensates for any mismatch between the two cells that may cause one of the cells to overcharge.

The balun ensures that SECBAL remains close to $V_{BAT}/2$. This configuration must be used if the dual battery supercapacitor is connected on the SECBAT .

11 Chip Configuration

11.1 LDO Related Configuration

11.1.1 Predefined Schemas

The predefined mode, by configuring three pins (VCF[2:0]), the user can set a specified working mode, which can meet the requirements of most application scenarios. For related configurations, please refer to Table 11-1 .

Table 11-1 Configuration application of VCF[2:0]

Configuration Pins			Energy Storage Device Voltage			LDO Output Voltage		V_{MPP} / V_{OV}
VCF[2]	VCF[1]	VCF[0]	V_{OC}	V_{CR}	V_{OD}	V_H	V_L	
1	1	1	4.12V	3.67V	3.60V	3.3V	1.8V	Li-ion battery
1	1	0	4.12V	4.04V	3.60V	3.3V	1.8V	Solid state Battery
1	0	1	4.12V	3.67V	3.01V	2.5V	1.8V	Li-ion/NiMH Battery
1	0	0	2.70V	2.30V	2.20V	1.8V	1.2V	Single core Super-Cap
0	1	1	4.50V	3.67V	2.80V	2.5V	1.8V	Dual core Super-Cap
0	1	0	4.50V	3.92V	3.60V	3.3V	1.8V	Dual core Super-Cap
0	0	1	3.63V	3.10V	2.80V	2.5V	1.8V	LiFePO4 battery
0	0	0	Custom mode, configurable through R1~R6				1.8V	

Three voltage threshold levels are defined as:

- V_{OC}: the maximum acceptable voltage on the energy storage element.
- V_{CR}: After a cold start, the minimum voltage required on the energy storage element before enabling the LDO.

- V_{OD}: The minimum voltage acceptable to the primary battery before switching to the primary battery or entering the shutdown state.

After selecting a predefined configuration, the resistor pins dedicated to the custom configuration should be left floating (OCCFG, CRCFG, ODCFG, FBHV). Custom mode allows user to define V_{OC}, V_{CR}, V_{OD} and V_H threshold voltages.

11.1.2 Custom Mode

In the custom mode, configure VCF[2:0] to be grounded, and the 6 configurable resistors need to be connected according to Figure 11-1 . The configuration calculation formula is as follows:

(1) V_{OC}, V_{CR}, V_{OD} are configured by R1~R4, if RT=R1+R2+R3+R4, then R1~R4 can be calculated according to the following formula:

- 1 MΩ ≤ RT ≤ 100 MΩ
- R1=RT (1V/ V_{OC})
- R2=RT(1V/ V_{CR} - 1V/ V_{OC})
- R3=RT(1V/ V_{OD} - 1V/V_{CR})
- R4=RT(1 - 1V/ V_{OD})

(2) V_H Configured by R5~R6, if RV=R5+R6, then R5 and R6 can be calculated according to the following formula:

- 1 MΩ ≤ RV ≤ 40 MΩ
- R5=RV(1V/ V_H)
- R6=RV(1 - 1V/ V_H)

(3) The resistance value should be selected as large as possible so that the excess power consumption is negligible. In addition, the configuration should comply with the following constraints to ensure the normal function of the chip.

- V_{CR} + 0.05V ≤ V_{OC} ≤ 4.5V
- V_{OD} + 0.05V ≤ V_{CR} ≤ V_{OC} - 0.05V
- 2.2V ≤ V_{OD}
- V_H ≤ V_{OD} -0.3V

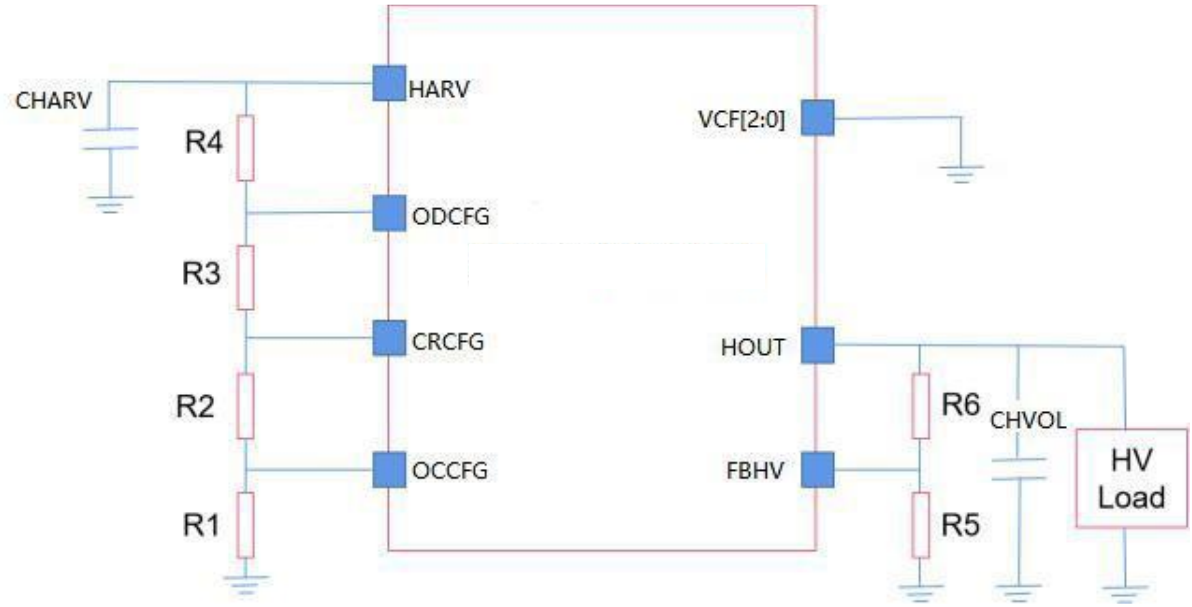


Figure 11-1 Schematic diagram of custom configuration connection

11.2 MPPT Configuration

Two dedicated configuration pins, MPPT[1:0], allow selection of the MPP tracking ratio according to the characteristics of the input source , as shown in Table 10-2.

11.3 Primary Battery Configuration

When using a primary battery, you must determine VPRIMBAT_MIN, which is the voltage used to judge that the primary battery is exhausted. Currently, you need to connect FBPD to GND. When the primary battery is not used, FBPD is kept floating to avoid quiescent current on the resistor. If RP=R7+R8, then R7 and R8 can be calculated according to the following formula:

- 100kΩ _ ≤RP≤500kΩ _ _ _ _
- R7=(VPRIMBAT_MIN/4) RP (1/2.2V)
- R8=RP-R7

11.4 Cold Start Configuration

Through the FBCD pin, the minimum cold crank voltage can be set above 400mV. Adding a resistor divider between SPW and GND sets the FBCD pin at the desired cold crank voltage. If RC=R9+R10, and define the new cold start voltage as VCS, then R9 and R10 can be calculated according to the following formula:

- 100kΩ _ ≤ RC ≤ 10MΩ _
- R9=0.38V (RC/VCS)
- R10=RC-R9

11.5 No Battery Configuration

If light energy collected from the environment is permanently available and meets the needs of the application, or if no energy storage is required when no light energy can be collected, an external capacitor CSECBAT with a minimum of 150μF can be used instead of the energy storage element.

11.6 Configuration of Energy Storage Components

The GW4235 can be a rechargeable battery, a supercapacitor or a large capacitor (minimum 150μF), and the voltage should not drop below V_{OD} even when the load current occasionally peaks. The leakage current of the capacitor should be as small as possible, because the leakage current directly affects the quiescent current of the subsystem. When selecting energy storage components, attention should be paid to:

(1) The CSPW capacitor acts as an energy buffer at the input of the boost converter, it can prevent large voltage fluctuations when the boost converter switches, the recommended value is 10μF+/- 20%

(2) The CHARV capacitor is used as an energy buffer for the boost converter, which can reduce the voltage ripple caused by the current pulse inherent in the switch mode of the converter, and the recommended value is 22μF +/- 20%

(3) The CHVOL and CLVOL capacitors ensure efficient load regulation for high-voltage and low-voltage LDO regulators. Closed-loop stability requires this value to be in the range of 8μF to 14μF.

12 Typical Application

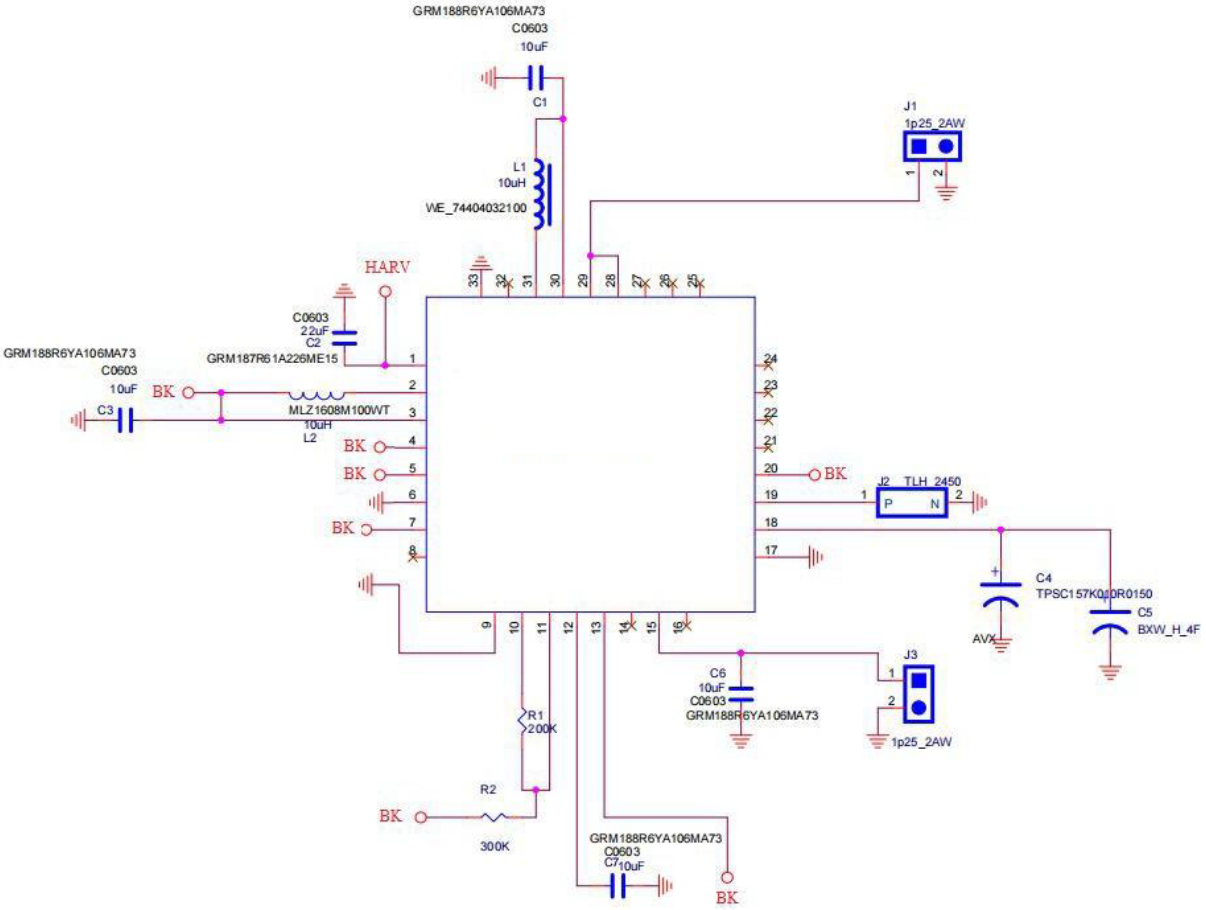


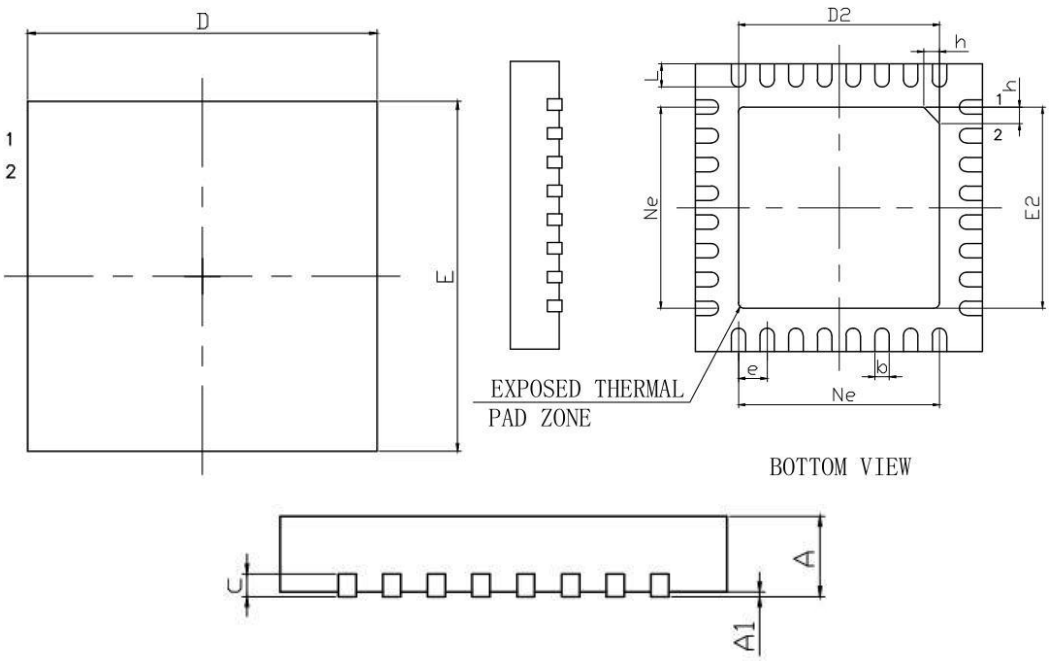
Figure 12-1 Typical application circuit

Typical application example, as shown in Figure 12-1, this application scenario is a typical wireless communication application scenario, the energy source is a photovoltaic cell, and the energy storage element can be a standard lithium battery or a super capacitor. The wireless communication module is powered by a 3.3V power supply, The microcontroller is powered by a 1.8V supply.

The circuit uses a predefined working mode, the working mode pin is connected to VCF[2:0]=110, refer to Table 10-1. In this mode, the threshold voltages are V_{OC} = 4.12V, V_{CR} = 4.04V, V_{OD} = 3.60V. At this point, the output voltage of the LDO is V_H = 3.3V, V_L = 1.8V. This solution uses the connection of a primary battery as a backup solution, and through the coordination of the resistance of R1 and R2 , the minimum level allowed by the battery is set to 3.5V. If you need to set the minimum level allowed by the battery to other voltage values, you can set it by modifying the resistance of R1 and R2, for example, R1=100KΩ, R2=300KΩ, then the minimum level allowed by the battery is set to 2.2V.

13 Package Information

5.0mmx5.0mm 0.5mm pitch package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	4. 90	5. 00	5. 10
D2	3. 40	3. 50	3. 60
e	0. 50BSC		
Ne	3. 50BSC		
E	4. 90	5. 00	5. 10
E2	3. 40	3. 50	3. 60
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40

Figure 13-1 Schematic diagram of chip packaging

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